REMARKS/ARGUMENTS

Claims 1-22 were previously pending in the application. Claim 4 is canceled; claims 1, 5, 14, 18, and 21 are amended; and new claims 23-30 are added herein. Assuming the entry of this amendment, claims 1-3 and 5-30 are now pending in the application. The Applicant hereby requests further examination and reconsideration of the application in view of the foregoing amendments and these remarks.

In paragraph 2, the Examiner rejected claims 1-3 and 8-22 under 35 U.S.C. § 102(b) as being anticipated by Murray. In paragraph 6, the Examiner rejected claims 4-7 under 35 U.S.C. § 103(a) as being unpatentable over Murray in view of Vaziri.

Independent claim 1 is amended to include the recitations of claim 4 (now canceled). Independent claims 14, 18, and 21 are similarly amended. The specification is amended to correct inadvertent typographical errors. For the following reasons, the Applicant submits that all pending claims are allowable over the cited references.

Claims 1-3 and 5-30:

Amended claim 1 is directed to a device having a splitter adapted to receive an input signal corresponding to a duobinary sequence and generate a first copy and a second copy of the input signal. The device also has first and second comparators and a logic gate. The first and second comparators are adapted to receive the first and second copies, respectively, and generate first and second binary signals, and the logic gate is adapted to generate a third binary signal based on the first and second binary signals, wherein the third binary signal is a binary representation of the duobinary sequence.

Murray discloses a circuit designed to convert a duobinary signal into a binary signal (see, e.g., Fig. 1 and page 1, lines 3-5). In the rejection of previously pending claim 4, on page 3, the Examiner admitted that Murray does not teach a splitter. However, on page 4, the Examiner stated that:

> Vaziri et al. disclose in Figure 1, a duobinary to binary encoder circuit which is a high rate system in the order of 10 Gb/s and capable of processing the duobinary signals at a predetermined bandwidth (see col. 1 lines 16 and lines 30-37). Vaziri et al. further disclose a splitter that splits the duobinary analog signal (see col. 5, lines 15-21). ... Therefore, it would have been obvious to one having ordinary skill in the art to set the bit rate and splits the duobinary input signal and also increase the rate of processing of the converter as taught by Vaziri et al. to provide a converter less susceptible to interference or other forms of disturbances and still capable to operate at a higher frequency.

Vaziri discloses a circuit for converting an electrical binary signal into an optical duobinary signal (see, e.g., Fig. 1 and col. 5, lines 7-10). Therefore, the circuit of Vaziri is a binary-to-duobinary encoder circuit and not "a duobinary to binary encoder circuit" as stated by the Examiner in the above-cited portion of the rejection. As such, it is submitted that the Examiner mischaracterized the teachings of Vaziri and used them improperly to reject the claims.

In addition, the Applicant submits that it would not have been obvious to one of ordinary skill in the art to combine the circuits of Murray and Vaziri because these circuits have opposite functionality. More specifically, the circuit of Murray acts as a duobinary-to-binary converter while the circuit of Vaziri acts as a binary-to-duobinary converter. As such, the circuit of Vaziri would substantially reverse the conversion performed by the circuit of Murray, and vice versa. Thus, incorporation of the circuit of

Vaziri into the circuit of Murray, and vice versa, would destroy the circuit functionality. For this reason, the Applicant submits that the Examiner improperly combined the teachings of Murray and Vaziri.

Even if the combination of Murray and Vaziri were proper, which the Applicant does not admit, it is submitted that Murray and Vaziri, independently or in combination, do not teach or even suggest a splitter adapted to generate first and second copies of an input signal, wherein the input signal corresponds to a duobinary sequence.

As already indicated above, the Examiner admitted that Murray does not teach a splitter. Instead, Murray relies on a simple branched wire to feed the input signal into comparators CP1 and CP2 (see, e.g., Murray's Fig. 1). The Applicant submits that, in the absence of a splitter, operation of the circuit at relatively high bit rates would be severely impaired. For example, at these bit rates, impedance mismatches in the feeds to comparators CP1 and CP2 would result in multiple signal reflections. These reflections would produce signal distortions that, for all practical purposes, would render further signal processing in the comparators substantially impossible.

In contrast, a device of claim 1 has a splitter (e.g., wideband splitter **312** of Fig. 1), one purpose of which is to substantially avoid the above-indicated impedance-mismatch problems. When the frequency range (bandwidth) of a splitter is explicitly called out as, e.g., on page 5, lines 11-13, one skilled in the art understands that this specified frequency range is the range over which a matched impedance is provided. As a result, over that range, signal reflections are significantly reduced, thereby advantageously reducing signal distortions and enabling further signal processing in the comparators.

Vaziri teaches an optical waveguide splitter that is a part of a Mach-Zehnder (MZ) interferometer (see, e.g., Fig. 1 and col. 5, lines 10-15). The splitter of Vaziri is adapted to split, e.g., a continuous-wave (CW) optical carrier signal **14** generated by a laser **11** (Fig. 1 and col. 7, lines 6-9). Since carrier signal **14** is not modulated when it is applied to the optical waveguide splitter, the carrier signal does not correspond to any data sequence. As such, Vaziri does not teach or even suggest a splitter adapted to receive an input signal and generate a first copy and a second copy of the input signal, wherein the input signal corresponds to a duobinary sequence.

For all these reasons, the Applicant submits that claim 1 is allowable over the cited references. For similar reasons, the Applicant submits that claims 14, 18, and 21 are also allowable over the cited references. Since claims 2-3, 5-13, 15-17, 19-20, and 22-30 depend variously from claims 1, 14, 18, and 21, it is further submitted that those claims are also allowable over the cited references. The Applicant submits therefore that the rejections of claims under §§ 102 and 103 have been overcome.

Claims 5, 21, 29, and 30:

Each of claims 5, 29, and 30 further specifies that the splitter has a bandwidth of at least about $1/2T_b$, where T_b is a bit period corresponding to the input signal. Claim 21 recites an analogous limitation. The Applicant submits that Murray and Vaziri, independently or in combination, do not teach or suggest such a limitation. This fact provides additional reasons for the allowability of claims 5, 21, 29, and 30 over the cited references.

For high-speed circuit design, e.g., for multi-gigabit data rates, it is advantageous to have a relatively narrow bandwidth because the wider the bandwidth, the less feasible, more complex, and more expensive the splitter becomes. The specified bandwidth is based on an assessment of power spectral density for a duobinary signal that provides that most of the signal energy is confined within a bandwidth of about 1/2Tb. Therefore, the bandwidth limitation recited in claims 5, 21, 29, and 30 enables a

relatively inexpensive implementation of a reliable duobinary-to-binary converter circuit that is not taught or suggested in the prior art.

Claims 23, 25, and 27:

Claim 23 specifies that each of the first and second threshold voltages is a selected constant voltage. Claims 25 and 27 include analogous recitations. For example, in a representative embodiment of converter **308** (Fig. 3) corresponding to claim 23, 25, or 27, each of voltages V1 and V2 applied to comparators **314a** and **314b**, respectively, is a constant voltage selected as described on page 5, lines 21-24.

In contrast, Murray teaches that threshold (reference) voltages X and Y applied to comparators CP1 and CP2 (Murray's Fig. 1) are generated using a rectifier circuit. More specifically, voltages X and Y are derived from the rectified peak (highest and lowest) levels in the input signal (see, e.g., page 3, line 19, through page 4, line 2). As such, both threshold voltages X and Y vary with variations in the input signal and, therefore, are not constant voltages.

For one or more of the following reasons, it may be advantageous to have a selected constant threshold voltage over a threshold voltage derived via peak detection in the input signal.

For a modern high-speed transmission system having a relatively large number of high-speed links (i.e. a high-speed backplane system), inter-link crosstalk is an important issue. For example, due to the crosstalk, energy from one trace may be coupled into a different trace, e.g., through radio-frequency (RF) emission. This coupling may cause the signal peak levels in each link to change in an unpredictable manner depending on the signals in the other links. In the circuit of Murray, these peak variations would result in threshold-voltage variations that would likely induce decoding errors. Having a constant threshold voltage advantageously reduces this problem.

Furthermore, at relatively high bit rates (e.g., greater than about 40 Gb/s), the design and implementation of a rectifier (peak detector) circuit of Murray becomes relatively difficult. More specifically, at these bit rates, parasitic RF couplings within the rectifier circuit may cause threshold-voltage changes even when the peak-to-peak amplitude swing in the input signal remains relatively steady. These changes would cause additional decoding errors. Having a constant threshold voltage provides a way of generating threshold voltages without the use of rectifier circuits, thereby reducing the number of decoding errors.

In summary, the Applicant submits that Murray does not teach or suggest that threshold voltages are selected constant voltages. This fact provides additional reasons for the allowability of claims 23, 25, and 27.

Claims 24, 26, and 28:

Claim 24 specifies that each of the first and second threshold voltages is not based on peak detection in the input signal. Claims 26 and 28 include analogous recitations. For example, in a representative embodiment of converter **308** (Fig. 3) corresponding to claim 24, 26, or 28, each of voltages V1 and V2 applied to comparators **314a** and **314b**, respectively, is not based on peak detection in input signal *S(t)*.

As already explained above, Murray does teach that threshold (reference) voltages X and Y applied to comparators CP1 and CP2 are generated based on peak detection in the input signal with a

rectifier circuit (see, e.g., page 3, line 19, through page 4, line 2). The Applicant submits that this fact provides additional reasons for the allowability of claims 24, 26, and 28.

In view of the above amendments and remarks, the Applicant believes that the now pending claims are in condition for allowance. Therefore, the Applicant believes that the entire application is now in condition for allowance, and early and favorable action is respectfully solicited.

Respectfully submitted,

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